SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester Supplementary Examinations December-2021
COMPUTER ORGANIZATION & ARCHITECTURE
(Common to CSE & CSIT)

Time: 3 hours | Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Write in detail about the Basic Operational Concepts with neat diagram.	L3	6M
	b	Explain the Instruction Cycle with neat diagram.	L4	6M

OR

2		Illustrate any four addressing modes with neat sketch.	L3	12M

UNIT-II

3	Show the steps of signed operand multiplication with example?	L2	12M

OR

4	Describe the Floating point numbers, its operations and implementation.	L2	12M

UNIT-III

5	a	Examine the Bus transfer with neat diagram.	L3	6M
	b	Summarize the Register Representations and way it is used.	L5	6M

OR

6	a	What is Hardwired Control? Explain in detail with a neat diagram.	L4	8M
	b	Describe about 4-bit incrementer with suitable example?	L2	4M

UNIT-IV

7	What is Main Memory and what are the types in it? Explain in detail.	L4	12M

OR

8	a	Define Cache Memory? Explain in detail its mapping functions.	L3	8M
	b	Explain about hit and miss in the Cache memory?	L2	4M

UNIT-V

9	a	Describe the concept of Pipelining with clear example.	L2	8M
	b	Write the characteristics of Multiprocessor.	L3	4M

OR

10	Implement three types multiprocessor system with neat sketch.	L6	12M

*** END ***